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Common Flash Interface (CFI)

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COMMON FLASH INTERFACE (CFI)

Contents

Introduction

The Common Flash Interface (CFI) specification outlines a device and host system software interrogation handshake that allows specific software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specified flash device families. It allows flash vendors to standardize their existing interfaces for long-term compatibility.

COMMON FLASH INTERFACE (CFI)

(From JEDEC Board Ballots JCB-98-81 and JCB-03-42, formulated under the cognizance of the JC-42.4 Subcommittee on Novolatile Memories)

1 Scope

This release of the specification defines the basic Query interface for CFI-compliant devices. This allows parameterization of known and future flash Read/Write/Program/Erase control interfaces. This Query structure attempts to define all the critical parameters relevant to a broad base of flash memory devices. The CFI specification will not specify detail command sets, status polling methods, and software algorithms of individual flash vendors. A 16-bit ID code is assigned to specific algorithm interfaces, and it is up to the algorithm manufacturers to provide these detailed specifications.

2 Overview

2.1 Operational summary

After the Query command code has been issued, the device enters the Query mode, allowing reads out of the CFI Query data structure. The CFI Query data structure contains a 16-bit Command Set and Control Interface ID code that specifies an algorithm-specific control interface for a family of flash devices. Query also contains general, common flash memory parameters and algorithm-specified data areas. These provide all the necessary information for controlling Read/Write/Program/Erase operations of a particular family of flash devices according to a algorithm-specified interface. Any additional information not covered in the common CFI Query data structure is located in algorithm-specific extended Query Table 9 and Table 10, the address location(s) of which is (are) contained in the general CFI Query structure.

3 Hardware interface

3.1 Query command interface

The CFI Query structure is accessed similar to the existing “ID Mode” or “JEDEC ID” access for nonvolatile memories, but uses a different, non-conflicting command code. The Query access command is 98h, while the JEDEC ID mode access mode is 90h. The Query addressing is always relative to the device word (largest supported) with data always presented on the lowest order byte (D7 - D0 outputs).

3 Hardware interface (cont'd)

3.1 Query command interface (cont'd)

Nonvolatile memory devices are assumed to power up in a read-only state. Independent of that assumption, the Query structure contents must be able to be read at the specific address locations following a single system write cycle where: 1) a 98h Query command code is written to 55h address location within the device's address space (in maximum device buswidth), and 2) the device is in any valid read state, such as "Read Array" or "Read ID Data". Other device states may exist within a long sequence of commands or data input; such sequences must first be completed or terminated before the writing of the 98h Query command code will result in valid Query data structure output.

NOTE For devices wider than 8 bits, the valid Query access code has all zeroes (0's) in upper bytes of the data bus. Thus the 16-bit Query command code is 0098h and the 32-bit Query command code is 00000098h.

A CFI-compliant device must allow selection and deselection of the Query output mode to and from normal read array operation with a single command write cycle so that the desired data are accessible in the second of two active bus cycles, i.e., bus cycles in which the devices Chip Enable(s) are active.

Table 1 — Command write cycles for query select and deselect

Command	# of Cycles	First Bus Cycle			Second Bus Cycle		
		Oper	Address	Data	Oper	Address	Data
Read Array	≥ 2	Write	X	FFh/F0h	Read	AA	AD
Query	≥ 2	Write	55h	98H	Read	QA	QD

NOTE 1 "Address" is the location in maximum device buswidth

NOTE 2 Flash devices may or may not have address sensitive query commands. Device drivers should always supply 55h on the address bus and 98h on the data bus to enter query mode; however Flash devices may choose to ignore the address bus and enter query mode if 98h is seen on the data bus only

NOTE 3 A flash vendor must define other command sequences for other mode accesses as part of the -specific Algorithm and Control Interface specification referenced by the appropriate CFI ID code. Access to and from Query and Read Array modes from any other mode may require additional command sequences.

NOTE 4 Abbreviations for inputs and outputs of the second cycle refer to address/data for the normal flash array (AA, AD) and Query structure (QA, QD), which may be accessed in random order.

3 Hardware interface (cont'd)

3.1 Query command interface (cont'd)

Table 2 — Summary of command sequence as a function of device and mode

Device type/ mode	Command location in maximum device buswidth addresses	Command data	Command address location in bytes	Command data with byte addressing
x8 device / x8 mode	55h	98h	55h	98h
x16 device / x16 mode	55h	0098h	AAh	AAh: 98h ABh: 00h
x16 device / x8 mode	N/A *	N/A *	AAh	AAh: 98h
x32 device / x32 mode	55h	00000098h	154h	154h: 98h 155h: 00h 156h: 00h 157h: 00h
x32 device / x8 mode	N/A *	N/A *	154h	154h: 98h

* The system must drive the lowest order addresses to access all the device's array data when the device is configured in x8 mode. Therefore, word addressing where these lower addresses are not toggled by the system is "Not Applicable" for x8-configured devices.

NOTE Flash devices may or may not have address sensitive query commands. Device drivers should always supply 55h on the address bus and 98h on the data bus to enter query mode; however Flash devices may choose to ignore the address bus and enter query mode if 98h is seen on the data bus only.

Table 3 — Example of query command sequence of a x8/x16 capable device with an address sensitive query command

Binary Address	-- x16 Mode (BYTE#=1) Address : Data	Binary Address	-- x8 Mode (BYTE#=0) Address : Data
$A_8A_7A_6A_5A_4A_3A_2A_1$	A_{16} - A_1 : D_{15} - D_0	$A_7A_6A_5A_4A_3A_2A_1A_0$	A_{15} - A_0 : D_7 - D_0
$A_7A_6A_5A_4A_3A_2A_1A_0$	A_{15} - A_0 : D_{15} - D_0	$A_6A_5A_4A_3A_2A_1A_0A_{-1}$	A_{14} - A_{-1} : D_7 - D_0
0 1 0 1 0 1 0 1	0055h : 0098h	1 0 1 0 1 0 1 0	00Aah : 98h

NOTE Address examples provided for devices with least significant byte address of A_0 or A_{-1}.

3 Hardware interface (cont'd)

3.2 Query structure output

Query data are always presented on the lowest-order data outputs (D7 - D0) only. The numerical offset value is the address relative to the maximum bus width supported by the device. The Query table device starting address is 10h byte address for a byte-wide (x8) device, 10h word address for word-wide (x16) device, 10h "dword" address for a x32 device, etc.

Thus for the bytewide (x8) device, the first 2 bytes of the Query structure, "Q" and "R" in ASCII, appear at device addresses 10h and 11h, which is the same as the absolute byte address. These same data appear on the low byte at word addresses 10h and 11h in a wordwide (x16) device. A CFI-compliant device must output 00H data on upper bytes. Thus, a x16 device outputs ASCII "Q" in the low byte (D7-D0) and 00h in the high byte (D15-D8). The same logic extends to x32 and larger devices, such that: 1) the data are presented in the lowest byte, 2) the data are addressed in maximum-buswidth-relative addresses, and 3) the upper bytes in each data word are filled with 00h data. Thus outputs D31 - D8 of a x32 device present 00h data during Query read, starting at word address 10h or byte-relative address 40h.

In devices that are x8/x16 capable, the x8 data is still presented in word-relative (16-bit) addresses. However, the "fill data" (00h) is not the same as driven by the upper bytes in the x16 mode. As in x16 mode, the byte address (A_0 or A_{-1} depending on pinout) is ignored for Query output so that the "odd byte address" (A_0 or A_{-1} high) repeats the "even byte address" data (A_0 or A_{-1} low). Therefore, in x8 mode using byte addressing, such devices will output the sequence "Q", "Q", "R", "R", "Y", "Y", and so on, beginning at byte-relative address 20h (which is equivalent to word offset 10h in x16 mode). Again, this is extensible to x32 and wider devices in that byte addresses are ignored during Query output in x8 mode such that: 1) Query data appears to repeat at each byte address within a word, and 2) the Query data starts at the byte address 10h times the number of bytes of maximum device buswidth.

3 Hardware interface (cont'd)

3.2 Query structure output (cont'd)

Table 4 — Summary of query structure output as a function of device and mode

Device type / mode	Query start location in maximum device buswidth addresses	Query data with maximum device buswidth addressing "x" = ASCII equivalent	Query start address in bytes	Query data with byte addressing
x8 device /x8 mode	10h	10h: 51h "Q" 11h: 52h "R" 12h: 59h "Y"	10h	10h: 51h "Q" 11h: 52h "R" 12h: 59h "Y"
x16 device / x16 mode	10h	10h: 0051h "Q" 11h: 0052h "R" 12h: 0059h "Y"	20h	20h: 51h "Q" 21h: 00h null 22h: 52h "R"
x16 device / x8 mode	N/A *	N/A *	20h	20h: 51h "Q" 21h: 51h "Q" 22h: 52h "R"
x32 device / x32 mode	10h	10h: 00000051h "Q" 11h: 00000052h "R" 12h: 00000059h "Y"	40h	40h: 51h "Q" 41h: 00h null 42h: 00h null 43h: 00h null 44h: 52h "R"
x32 device / x8 mode	N/A *	N/A *	40h	40h: 51h "Q" 41h: 51h "Q" 42h: 51h "Q" 43h: 51h "Q" 44h: 52h "R"

* The system must drive the lowest order addresses to access all the device's array data when the device is configured in x8 mode. Therefore, word addressing where these lower addresses are not toggled by the system is "Not Applicable" for x8-configured devices.

3 Hardware interface (cont'd)

3.2 Query structure output (cont'd)

Table 5 — Example of query structure output of a x8/x16 capable device

Binary Address	-- x16 Mode (BYTE# =1) Address : Data		Binary Address	-- x8 Mode (BYTE# =0) Address : Data	
$A_6A_5A_4A_3A_2A_1$	A_{16} - A_1 : D_{15} - D_0		$A_5A_4A_3A_2A_1A_0$	A_7 - A_0 : D_7 - D_0	
$A_5A_4A_3A_2A_1A_0$	A_{15} - A_0 : D_{15} - D_0		$A_4A_3A_2A_1A_0A_{-1}$	A_6 - A_{-1} : D_7 - D_0	
0 1 0 0 0 0	0010h: 0051h	"Q"	1 0 0 0 0 0	20h: 51h	"Q"
0 1 0 0 0 1	0011h: 0052h	"R"	1 0 0 0 0 1	21h: 51h	"Q"
0 1 0 0 1 0	0012h: 0059h	"Y"	1 0 0 0 1 0	22h: 52h	"R"
0 1 0 0 1 1	0013h: P_ID_{LO}	PrAlgo ID# (lo)	1 0 0 0 1 1	23h: 52h	"R"
0 1 0 1 0 0	0014h: P_ID_{HI}	PrAlgoID# (hi)	1 0 0 1 0 0	24h: 59h	"Y"
0 1 0 1 0 1	0015h: P_ADR_{LO}	PrAlgo TblAdr (lo)	1 0 0 1 0 1	25h: 59h	"Y"
0 1 0 1 1 0	0016h: P_ADR_{HI}	PrAlgo TblAdr (hi)	1 0 0 1 1 0	26h: P_ID_{LO}	PrAlgo ID# (lo)
0 1 0 1 1 1	0017h: A_ID_{LO}	AltAlgo ID# (lo)	1 0 0 1 1 1	27h: P_ID_{LO}	PrAlgo ID# (lo)
0 1 1 0 0 0	0018h: A_ID_{HI}	AltAlgo ID# (hi)	1 0 1 0 0 0	28h: P_ID_{HI}	PrAlgo ID# (hi)
		…	...	...	

NOTE Address examples provided for devices with least significant byte address of A_0 or A_{-1}.

3.3 Query structure

3.3.1 Query structure overview

The Query command causes the flash component to display the CFI Query structure or "database." The structure sub-sections and address locations are summarized as follows:

Offset	Sub-section Name	Description
00h	*Reserved*	*Reserved for algorithm-specific information*
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
P	Primary Algorithm-specific Extended Query (Table 9)	Additional information specific to the Primary Algorithm *(optional)*
A	Alternative Algorithm-specific Extended Query (Table 10)	Additional information specific to the Alternate Algorithm *(optional)*

The following sections describe the Query structure sub-sections in detail.

3.3 Query structure (cont'd)

3.3.2 Query identification string

The Identification String provides verification that the component supports the Common Flash Interface specification. Additionally, it indicates which version of the specification and which Algorithm-specific command set(s) is(are) supported.

Table 6 — Identification string

Offset	Length (bytes)	Description
10h	03h	Query-unique ASCII string "QRY"
13h	02h	Primary Algorithm Command Set and Control Interface ID Code 16-bit ID code defining a specific algorithm. (Ref. JEP137)
15h	02h value = ***P***	Address for Primary Algorithm extended Query, Table 9 NOTE — Address 0000h means that no extended table exists.
17h	02h	Alternative Algorithm Command Set and Control Interface ID Code second specific algorithm supported by the device. (Ref. JEP137) NOTE — ID Code = 0000h means that no alternate algorithm is employed.
19h	02h value = ***A***	Address for Alternative Algorithm extended Query, Table 10 NOTE — Address 0000h means that no alternate extended table exists.

NOTE 1 Refer to Query Structure Output section of CFI Hardware Interface for the detailed definition of offset address as a function of device wordwidth and mode.

NOTE 2 The CFI specification allows for replacement of all or part of the standard Query table contents. If the Primary (or Alternative) Algorithm extended Query, see Table 9 and Table 10, address (P or A) points to any address between 10h and the end of the Flash Geometry, see Table 8, the standard Query table contents from that point on are assumed to be replaced by the information defined by the Primary (or Alternative) Algorithm. Thus, some or all of the standard Query may be replaced. For example, a Primary (or Alternative) Algorithm extended Query, see Table 9 and Table 10, address of 27h means that the standard Device Geometry definition has been replaced by something which has been defined by the Algorithm. The System Interface information at locations 1Bh to 26h may be assumed valid, but the ultimate definition must be described by the particular algorithm. If the Primary (or Alternative) Algorithm extended Query, Table 9 and Table 10, address points to an address beyond the end of the Flash Geometry, see Table 8, a new table of data is included at that address. The contents of Table 8 are defined by the corresponding Primary (or Alternative) Algorithm.

3.3 Query structure (cont'd)

3.3.3 Query system interface information

The following device information can be useful in optimizing system interface software.

Table 7 — Device-system interface

Offset	Length (bytes)	Description
1Bh	01h	Vcc Logic Supply Minimum Program/Erase or Write voltage bits 7 - 4 BCD value in volts bits 3 - 0 BCD value in 100 millivolts
1Ch	01h	Vcc Logic Supply Maximum Program/Erase or Write voltage bits 7 - 4 BCD value in volts bits 3 - 0 BCD value in 100 millivolts
1Dh	01h	Vpp [Programming] Supply Minimum Program/Erase voltage bits 7 - 4 HEX value in volts bits 3 - 0 BCD value in 100 millivolts Note: This value must be 00h if no Vpp pin is present
1Eh	01h	Vpp [Programming] Supply Maximum Program/Erase voltage bits 7 - 4 HEX value in volts bits 3 - 0 BCD value in 100 millivolts Note: This value must be 00h if no Vpp pin is present
1Fh	01h	Typical timeout per single byte/word/D-word program (multi-byte program count = 1), 2^N µs (if supported; 00h = not supported)
20h	01h	Typical timeout for maximum-size multi-byte program, 2^N µs (if supported; 00h = not supported)
21h	01h	Typical timeout per individual block erase, 2^N ms (if supported; 00h = not supported)
22h	01h	Typical timeout for full chip erase, 2^N ms (if supported; 00h = not supported)
23h	01h	Maximum timeout for byte/word/D-word program, 2^N times typical (offset 1Fh) (00h = not supported)
24h	01h	Maximum timeout for multi-byte program, 2^N times typical (offset 20h) (00h = not supported)
25h	01h	Maximum timeout per individual block erase, 2^N times typical (offset 21h) (00h = not supported)
26h	01h	Maximum timeout for chip erase, 2^N times typical (offset 22h) (00h = not supported)

3.3 Query structure (cont'd)

3.3.4 Device geometry definition

This field provides critical details of the flash device geometry.

Table 8 — Flash geometry

Offset	Length (bytes)	Description
27h	01h	Device Size = 2^n in number of bytes.
28h	02h	Flash Device Interface Code description (Ref. JEP137)
2Ah	02h	Maximum number of bytes in multi-byte program = 2^n.
2Ch	01h	Number of Erase Block Regions within device **bits 7-0 = x** = number of Erase Block Regions NOTE 1 x = 0 means no erase blocking, i.e. the device erases at once in "bulk." NOTE 2 x specifies the number of regions within the device containing one or more contiguous Erase Blocks of the same size. For example, a 128 KB device (1 Mb) having blocking of 16 KB, 8 KB, four 2 KB, two 16 KB, and one 64 KB is considered to have 5 Erase Block Regions. Even though two regions both contain 16 KB blocks, the fact that they are not contiguous means they are separate Erase Block Regions. NOTE 3 By definition, symmetrically block devices have only one blocking region.
2Dh	04h	Erase Block Region Information **bits 31- 16 = z**, where the Erase Block(s) within this Region are (z) times 256 bytes in size. The value z = 0 is used for 128-byte block size. e.g., for 64KB block size, z = 0100h = 256 => 256 * 256 = 64 K **bits 15 - 0 = y**, where y+1 = Number of Erase Blocks of identical size within the Erase Block Region: e.g., y = D15-D0 = FFFFh => y + 1 = 64 K blocks [maximum number] y = 0 means no blocking (# blocks = y+1 = "1 block") NOTE y = 0 value must be used with # of block regions of one as indicated by (x) = 0
31h - (k-1)h	04h per entry	Additional Erase Block Region Information, 4 bytes per region NOTE 1 The total number of blocks times individual block size must add up to the device size. NOTE 2 The address K is the next available Query address at the end of the Device Geometry structure. It is the first possible starting address of the optional algorithm-specific Query in Table 9 and Table 10 (i.e., Address "P," the Primary Algorithm extended Query, Table 9, offset, must be ≥ k to not overwrite the existing tables). See note 2 under Table 2 for more information.

3.3 Query structure (cont'd)

3.3.5 Optional algorithm-specific extended

3.3.5.1 Query tables

Certain flash features and commands may be optional in a specific algorithm specification. The optional algorithm-specific Query, Table 9 and Table 10, may be used to specify this and other types of information. These structures are defined solely by the flash vendor(s).

Table 9 — Primary algorithm-specific extended query

Offset	Length (bytes)	Description
(P)h	03h	Primary Algorithm extended Query table unique ASCII string "PRI"
(P+3)h	01h	Major version number, ASCII
(P+4)h	01h	Minor version number, ASCII
(P+5)h	variable	Extended Query, table contents for Primary Algorithm

Table 10 — Alternative algorithm-specific extended query

Offset	Length (bytes)	Description
(A)h	03h	Alternative Algorithm extended Query table unique ASCII string "ALT"
(A+3)h	01h	Major version number, ASCII
(A+4)h	01h	Minor version number, ASCII
(A+5)h	variable	Extended Query table contents for Alternate Algorithm

4 Extensibility

The CFI specification supports extensibility for future device characteristics through the algorithm-specific extended Query, Table 9 and Table 10. Anything not defined in the common CFI Query database is to be defined in the algorithm extended tables, with the detailed structure of such tables defined by the major and minor algorithm revision numbers and the associated vendor-supplied Command Set and Control Interface specification.

Annex A (informative) **Differences between JESD68.01 and JESD68**

This table briefly describes most of the changes made to entries that appear in this publication, JESD68.01, compared to its predecessor, JESD68 (September 1999). If the change to a concept involves any words added or deleted, it is included. Punctuation changes may not be included.

Page	**Description of change**
Page 8	In table 7, for Offset 1Fh added ‘D-word’ to description.
Page 8	In table 7, for Offset 23h added ‘D-word’ to description.

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